Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.064”**

**.072”**

**6 5 4 3 2**

**1**

**16**

**11 12 13 14 15**

**7**

**8**

**9**

**10**

**MASK**

**REF**

**TCH**

**367T**

**Top Material: Si**

**Backside Material: Al**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: HCT367T**

**APPROVED BY: DK DIE SIZE .064” X .072” DATE: 8/26/21**

**MFG: TEXAS INSTRUMENTS THICKNESS .012” P/N: 54HCT367**

**DG 10.1.2**

#### Rev B, 7/19/02